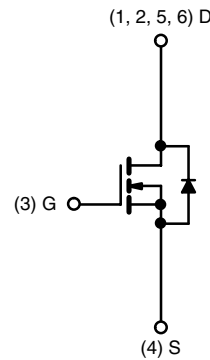
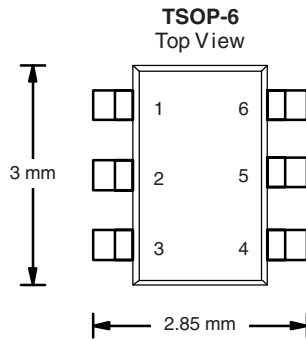


N-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.057 at $V_{GS} = 4.5$ V	4.2
	0.090 at $V_{GS} = 2.5$ V	3.4



RoHS
COMPLIANT



Ordering Information: Si3442BDV-T1-E3 (Lead (Pb)-free)

Marking Code: 2Bxxx

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V_{DS}	20		V	
Gate-Source Voltage	V_{GS}	± 12			
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	4.2	3.0	A
		$T_A = 70$ °C	3.4	2.4	
Pulsed Drain Current	I_{DM}	20			
Continuous Source Current (Diode Conduction) ^a	I_S	1.4	0.72	W	
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	1.67		0.86
		$T_A = 70$ °C	1.07		0.55
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ s	75	100	°C/W
		Steady State	120	145	
Maximum Junction-to-Foot (Drain)	R_{thJF}	70	85		

Notes:

a. Surface Mounted on FR4 Board, $t \leq 5$ s.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.8	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 4.5\text{ V}$	10			A
		$V_{DS} = 5\text{ V}, V_{GS} = 2.5\text{ V}$	4			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$		0.045	0.057	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 3.4\text{ A}$		0.070	0.090	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 4.0\text{ A}$		11.3		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.6\text{ A}, V_{GS} = 0\text{ V}$		0.75	1.2	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		295		μF
Output Capacitance	C_{oss}			75		
Reverse Transfer Capacitance	C_{rss}			45		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.0\text{ A}$		3	5	nC
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			0.95		
Gate Resistance	R_g	$f = 1\text{ MHz}$		2.7		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 6\text{ }\Omega$		35	55	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}		$I_F = 1.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		30	

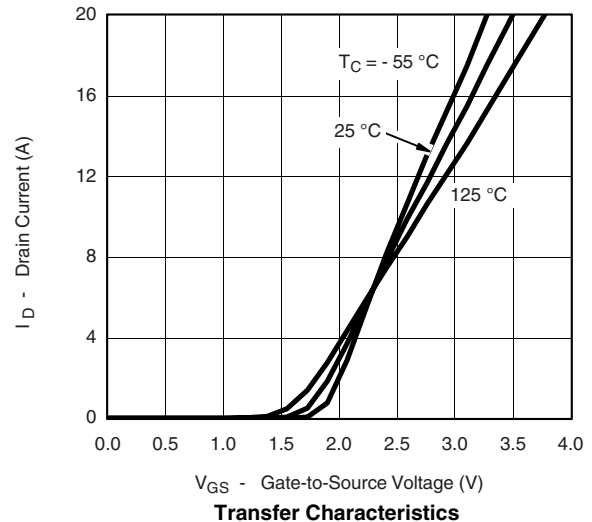
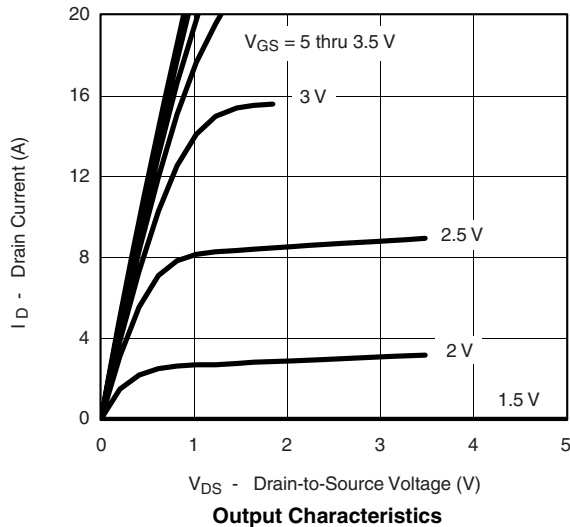
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

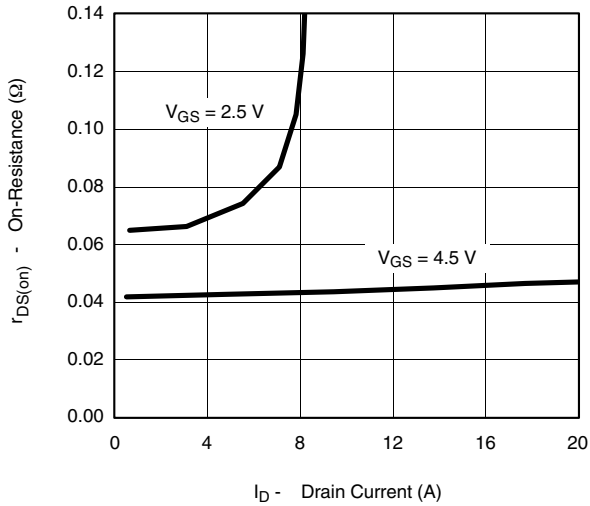
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

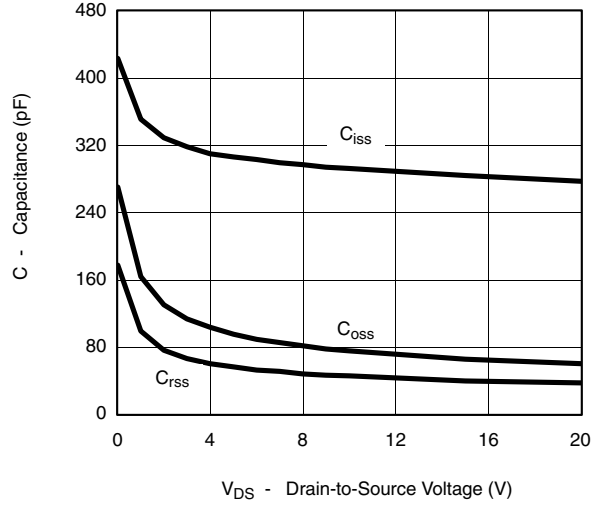
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



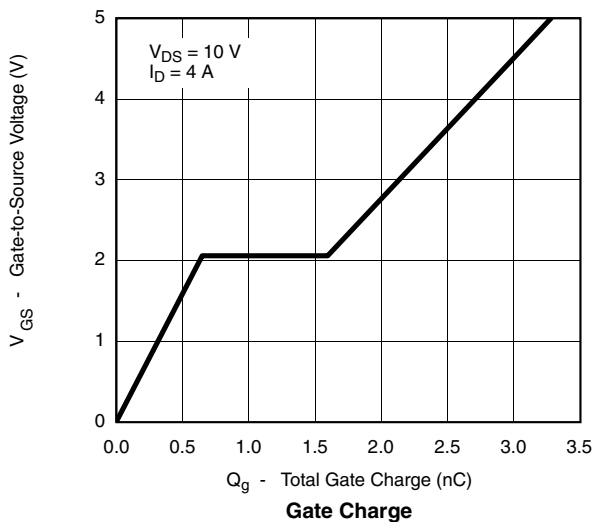
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



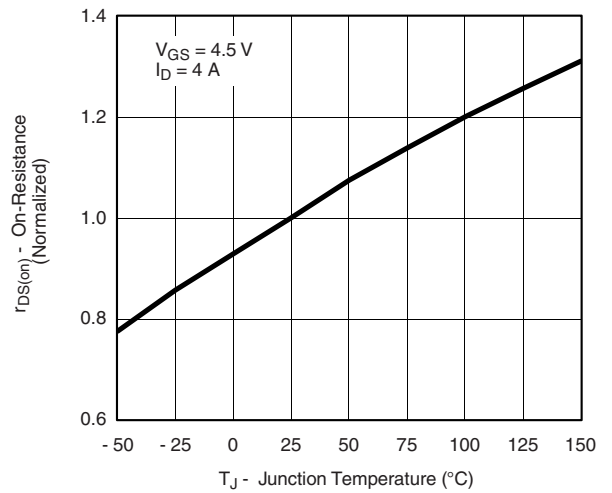
On-Resistance vs. Drain Current



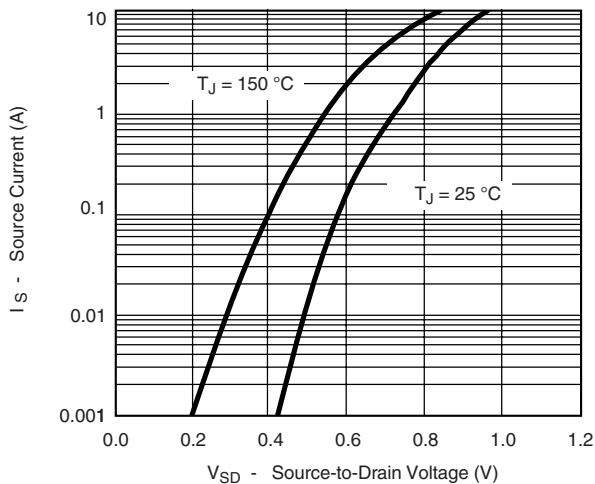
Capacitance



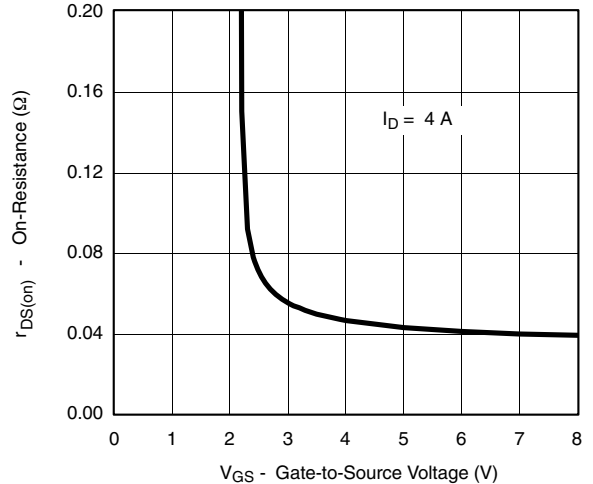
Gate Charge



On-Resistance vs. Junction Temperature

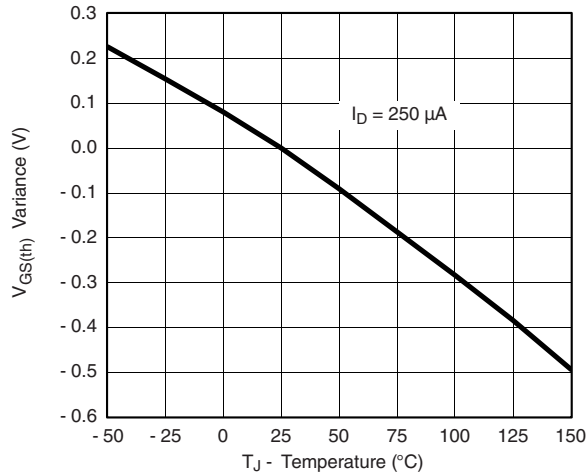


Source-Drain Diode Forward Voltage

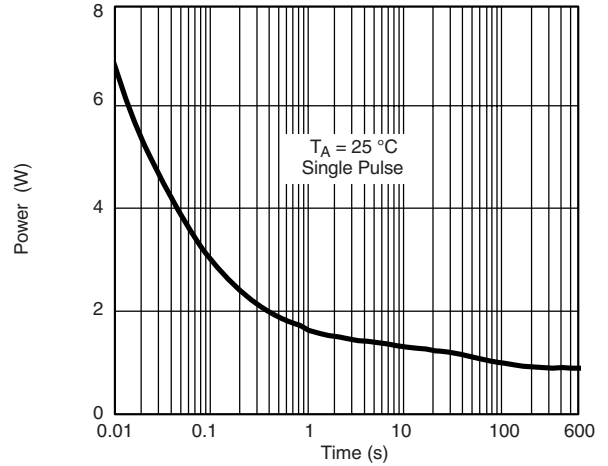


On-Resistance vs. Gate-to-Source Voltage

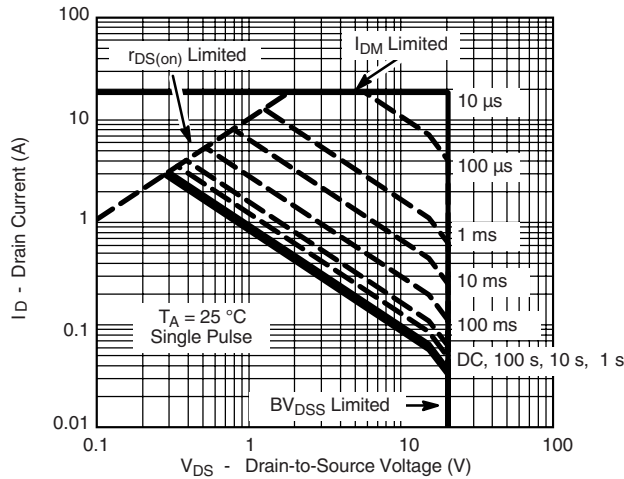
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



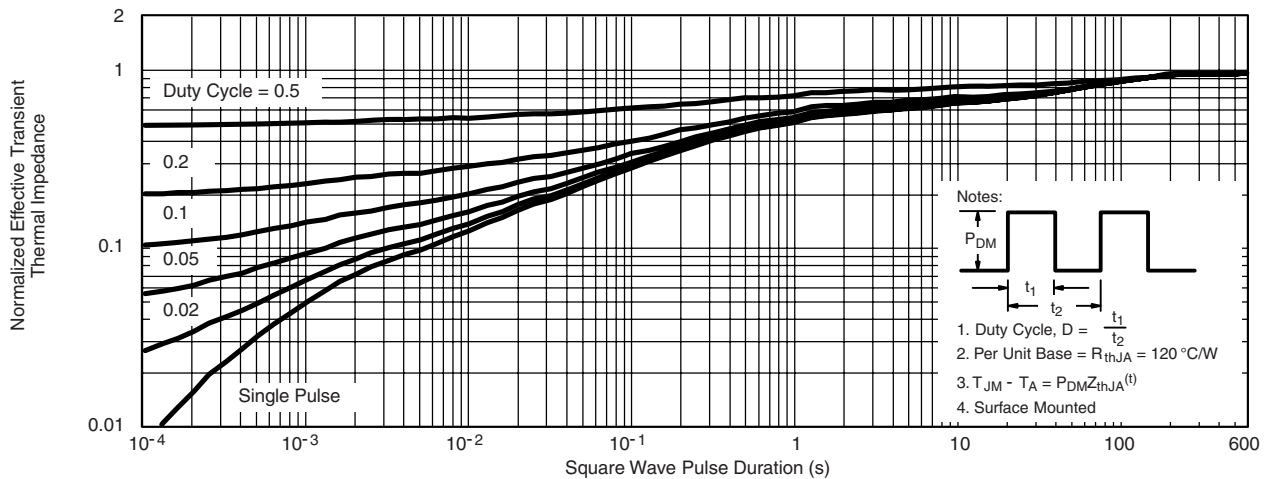
Threshold Voltage



Single Pulse Power



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

- Notes:
1. Duty Cycle, $D = \frac{t_1}{t_2}$
 2. Per Unit Base = $R_{thJA} = 120\text{ °C/W}$
 3. $T_{JM} - T_A = P_{DM}Z_{thJA}^{(t)}$
 4. Surface Mounted

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